

CIRCUIT BOARD HAVING THEREON COUPLED CERAMIC CAPACITORS  
AND METHOD FOR THE MANUFACTURE THEREOF

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Field of the Invention

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The present invention relates to a circuit board having thereon coupled multilayered ceramic capacitors capable of reducing generation of sounds caused by piezoelectric effects and a method for mounting the multilayered ceramic capacitors 10 on the circuit board.

Description of the Prior Art

15 Aluminum electrolysis capacitors had been widely used as power smoothing capacitors in smoothing circuits of such power supply circuits as DC-DC converters and the like.

However, as the sizes of electronic circuits and devices were scaled down, tantalum electrolysis capacitors, a smaller tantalum electrolysis capacitor being capable of providing a 20 capacitance level obtainable from a larger aluminum electrolysis capacitor, were employed in electronic circuits, e.g., smoothing circuits of power supply circuits, requiring large capacitance.

And, as the electronic circuits and devices are further 25 miniaturized while requiring less power consumption, most of the conventional capacitors employed therein have been rapidly

replaced by multilayered ceramic capacitors.

The use of multilayered ceramic capacitors have been rapidly extended since they are small but have excellent reliability and durability.

5 Since, however, a dielectric material being used in a multilayered ceramic capacitors having a small size but with large capacitance is of the type having a large dielectric constant, vibrations are generated due to piezoelectric effects when AC currents are applied thereto along with DC currents. The vibrations thus generated tend to become stronger as the dielectric constant of the dielectric material becomes greater and the size of the capacitor becomes larger.

10 Multilayered ceramic capacitors having relatively large sizes and large capacitance are normally employed in the 15 smoothing circuits of the power supply circuits, resulting in such vibrations occurring frequently.

Furthermore, once the vibrations are generated in the multilayered ceramic capacitors as described above, the vibrations of the capacitors are transferred to the circuit board on which the capacitors are mounted; and, therefore, in some cases the circuit board resonates with the vibrations so that sounds can be amplified. That is to say, the vibrations of the capacitors result in the vibration of the surrounding air to produce audible sounds and, at the same time, cause the 20 resonant vibrations of the circuit board to occur. Consequently, sound pressure levels increase, which in turn 25

results in harsh audible sounds being produced.

Summary of the Invention

5 It is, therefore, an object of the present invention to provide a circuit board capable of reducing audible sounds generated by piezoelectric effects and a method for mounting multilayered ceramic capacitors on the circuit board.

In accordance with one aspect of the present invention, 10 there is provided a circuit board having an electronic circuit formed thereon, the electronic circuit including a pair of multilayered ceramic capacitors, wherein each of the capacitors includes a body having dielectric layers formed of a dielectric ceramic material and internal electrode layers 15 and a pair of external terminal electrodes formed on two sides of the body, the body being of a substantially hexahedral shape, the dielectric layers and the internal electrode layers being stacked alternately in the body and the internal electrode layers being connected in parallel to the external 20 terminal electrodes in an alternate manner, characterized in that:

*Sub A<sup>2</sup>* ~~the capacitors are disposed at substantially plane-symmetrical positions on two opposite surfaces of the circuit board and substantially identical voltages are applied to the capacitors~~

~~In accordance with another aspect of the present~~

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invention, there is provided a method for mounting multilayered ceramic capacitors on a circuit board having a front surface and a back surface, wherein each capacitor includes a body having dielectric layers formed of a dielectric ceramic material and internal electrode layers and a pair of external terminal electrodes formed on two sides of the body, the dielectric layers and the internal electrode layers being stacked alternately in the body and the internal electrode layers being connected in parallel to the external terminal electrodes in an alternate manner, the method comprising the steps of:

15 forming lands at substantially plane-symmetrical positions on the front and the back surfaces, wherein every two lands disposed at their substantially plane-symmetrical positions are connected each other; and

mounting the capacitors on the lands of the front and the back surfaces such that the external terminal electrodes of the capacitors are electrically coupled to the lands on the front and the back surfaces.

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#### Brief Description of the Drawings

The above and other objects and features of the present invention will become apparent from the following description of preferred embodiments given in conjunction with the accompanying drawings, in which:

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Fig. 1 illustrates a perspective view of multilayered ceramic capacitors mounted on a circuit board in accordance with a preferred embodiment of the present invention;

5 Fig. 2 shows a cross sectional view of the multilayered ceramic capacitors mounted on the circuit board in accordance with the embodiment of the present invention;

10 Fig. 3 is a circuit diagram of a DC-DC converter incorporating therein the multilayered ceramic capacitors mounted on the circuit board in accordance with the embodiment of the present invention;

Fig. 4 presents a diagram for illustrating vibrations of the multilayered ceramic capacitors of the embodiment of the present invention; and

15 Figs. 5A and 5B represent waveforms of vibrations generated from two multilayered ceramic capacitors of the embodiment of the present invention, respectively.

#### Detailed Description of the Preferred Embodiments

20 A preferred embodiment of the present invention will now be described hereinafter with reference to the drawings.

Fig. 1 is a perspective view of a circuit board having a pair of multilayered ceramic capacitors mounted thereon and Fig. 2 is a cross sectional view thereof. In Figs. 1 and 2, 25 reference numerals 1A and 1B represent a pair of multilayered ceramic capacitors (referred to as capacitors hereinafter),

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each of which includes a body 13 formed by stacking dielectric layers 11 and internal electrodes 12 alternately, and a pair of external electrodes 14a and 14b disposed on two opposite sides of the body 13. The internal electrodes 12 are composed 5 of two sets of alternately disposed internal electrodes and the alternate internal electrodes of each set are connected to one of the external electrodes 14a and 14b in parallel.

Each of the dielectric layers 11 is made of a sintered ceramic in a form of a sheet having a substantially 10 rectangular shape, the sintered ceramic being a dielectric material having, e.g., magnesium titanate as the major component thereof.

Each of the internal electrodes 12 is formed of a metal film of a sintered metal paste, the metal paste being of a 15 type having, e.g., noble metals such as Pd, Ag-Pd or the like as the major component thereof. The external electrodes 14a and 14b can be made of a material identical to that of the internal electrodes 12 and provided with solderable plating layers on the surfaces thereof to improve solder wettability.

20 In the preferred embodiment of the invention, it is preferable that the capacitors 1a and 1b are identical each other.

However, the capacitors 1a and 1b may not be identical 25 each other but rather they can be constructed to be substantially identical each other, i.e., to be different in some aspects as long as the vibrations generated therefrom can

be substantially cancelled out by each other, as will be described hereinafter.

For example, the major factors controlling the degree of cancellation of the vibrations generated from the capacitors in actual use include an electromechanical coupling coefficient, a dielectric constant, a thickness of each layer, and the number of layers, etc. The preferable ranges of these factors required in effecting the cancellation of the vibrations have been obtained from experiments as follows:

10 An electromechanical coupling coefficient of one of the capacitors 1a and 1b being set to be in the range from about 70% to about 130% of that of the other capacitor.

15 A dielectric constant of a dielectric material used in one of the capacitors 1a and 1b being set to be in the range from about 50% to about 150% of that of the other capacitor.

20 A thickness of each layer in one of the capacitors being set to be in the range from about 70% to about 130% of that of the other capacitor in case the number of layers of one of the capacitors 1a and 1b is set to be substantially equal to that of the other capacitor.

25 The number of layers of one of the capacitors being set to be in the range from about 70% to about 130% of that of the other capacitor in case a thickness of each layer in one of the capacitors 1a and 1b is substantially equal to that of the other capacitor.

The dimensions, i.e., the length, the width and the

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height of one of the capacitors being set to be in the range from about 70% to about 130% of those of the other capacitor, respectively.

By using capacitors constructed satisfying the conditions 5 described above, vibrations generated therefrom can be substantially reduced.

Reference numeral 2 represents a circuit board, e.g., a single-layered double-sided printed circuit board with two mounting surfaces. Contact pads or lands 21a, 22a and 21b, 10 22b for mounting the capacitors 1a and 1b are formed on a front surface 2a and a back surface 2b of the circuit board 2, respectively. The lands 21a and 22a are in plane symmetry with the lands 21b and 22b, respectively, and the two lands in plane symmetry are electrically coupled to each other via 15 a through hole 23. That is, the land 21a formed on one side of the front surface 2a is electrically coupled to the land 21b formed on the back surface 2b via the through hole 23; and the land 22a formed on the other side of the front surface 2a is electrically coupled to the land 22b formed on the back 20 surface 2b via the through hole 23. It is to be understood that the circuit board 2 of the present invention can be different types of circuit boards, e.g., a multilayered ceramic circuit board or the like, other than the single-layered double-sided printed circuit board described above.

25 Interconnection between each pair of coupled lands, i.e., 21a, 21b and 22a, 22b, can be achieved by a combination of a

through hole and a wiring pattern, a jumper wiring or the like. That is, any type of interconnection schemes can be employed for the interconnection of each coupled lands as long as identical or substantially identical voltages can be  
5 applied to both the capacitors 1a and 1b.

The inventor of the present invention has found from experiments that the cancellation of the vibrations generated from the capacitors can be effected if the voltages applied to the two capacitors are substantially identical each other  
10 to satisfy certain criteria defined as follows:

That is, in the electronic circuit having the capacitors 1a and 1b, it is required that a voltage applied to one of the capacitors 1a and 1b be within the range from about 80% to about 120% of that applied to the other capacitor.

15 In the electronic circuit, a phase offset or difference of a voltage applied to one of the capacitors 1a and 1b with respect to that for the other capacitor is required to be less than about 20% of the phase period of the voltage applied to the other capacitor.

20 In the electronic circuit with the capacitors 1a and 1b to which DC bias voltages are applied, a DC bias voltage applied to one of the capacitors is required to be in the range from about 80% to about 120% of that applied to the other capacitor.

25 If substantially identical voltages satisfying any one of the conditions described above are applied to the

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capacitors 1a and 1b, vibrations being generated by the capacitors can be considerably reduced.

The external electrode 14a of the capacitor 1a mounted on the front surface 2a of the circuit board 2 is electrically coupled to the land 21a by solder and the other external electrode 14b thereof is electrically connected to the land 22a. Similarly, the external electrode 14a of the capacitor 1b mounted on the back surface 2b of the circuit board 2 is electrically connected to the land 21b by solder and the other external electrode 14b thereof is electrically connected to the land 22b.

In order to suppress the vibrations generated from the capacitors 1a and 1b, it is preferable that the capacitors 1a and 1b are mounted on the circuit board 2 in a manner of plane symmetry.

It is, however, virtually impossible to mount two capacitors 1a and 1b on the circuit board in their exactly plane-symmetrical positions. In view of the foregoing, the inventor conducted experiments to determine ranges of offset between the mounting positions of the capacitors which can substantially prevent the vibrations from being generated from the capacitors; and found that the preferable offset ranges between two capacitors mounted on substantially plane-symmetrical positions, which can effect the cancellation of the vibrations, are as follows.

That is, a mounting position of one of the capacitors is

required to be displaced from that of the other capacitor such  
that offsets of the one of the capacitors along directions of  
a length and a width of the other capacitor are not greater  
than about 30% of the length and the width of the other  
5 capacitor, respectively.

Further, the angle between the center axes along the length directions of the two capacitors mounted on substantially plane-symmetrical positions is required not to be greater than 40 degree.

10 Referring to Fig. 3, there is illustrated an exemplary electronic circuit in accordance with the embodiment of the invention.

Fig. 3 represents a circuit for illustrating a DC-DC converter 30 including therein the capacitors 1a and 1b mounted on a circuit board in a manner described above. In 15 Fig. 3, reference numerals 31, 32, 33, 34 and 35 represent a DC power supply, a P channel FET, a pulse width modulation circuit, a diode and an inductor, respectively, and reference numerals 1a and 1b are the capacitors described above.

20 A positive terminal of the DC power supply 31 is connected to a source of the FET 32. A drain of the FET 32 is connected to a cathode of the diode 34 and also connected to one external electrode of each of the capacitors 1a and 1b and an output terminal 36a via the inductor 35. An anode of 25 the diode 34 and the other external electrode of the capacitors 1a and 1b are connected to a negative terminal of

the DC power supply 31 and an ground terminal 36b. A voltage  $V_{con}$  outputted from the pulse width modulation circuit 33 is fed to a gate of the FET 32.

The pulse width modulation circuit 33 outputs the voltage 5  $V_{con}$  having a pulse width  $t$  with a predetermined period  $T$ . When the voltage  $V_{con}$  is applied to the gate of the FET 32, the FET 32 turns on so that the source and the drain of the FET 32 can be electrically connected each other.

When the FET 32 is on, the source-to-drain current is 10 outputted to the output terminal 36a via the inductor 35. The current is also fed to and charges the capacitors 1a and 1b.

When the FET 32 is off, the current from the DC power supply 31 is blocked by the FET 32; and then the energy accumulated in the inductor 35 discharges by a counter electromotive force and a freewheeling current due to the 15 counter electromotive force flows through the diode 34 and the capacitors 1a and 1b and to the output terminal 36a.

The output voltage  $V_o$  on the output terminal 36a can be represented by an output voltage  $V_{in}$  of the DC power supply 31 20 as follows:

$$V_o = V_{in} \frac{t}{T} .$$

That is, the voltage  $V_o$  is obtained by multiplying the voltage  $V_{in}$  by the pulse width  $t$  divided by the period  $T$ . Therefore, the output voltage  $V_o$  may be arbitrarily adjusted

by changing the ratio of the pulse width  $t$  to the period  $T$  in the pulse width modulation circuit 33.

Since the capacitors 1a and 1b serve to regulate or smooth the output of the DC-DC converter circuit 30, they need 5 be of a large capacitance. Further, besides a DC voltage, an AC voltage is also applied to the capacitors 1a and 1b, resulting in the vibrations of the capacitors 1a and 1b due to piezoelectric effects.

Since, however, the capacitors 1a and 1b of the embodiment of the present invention are mounted on the surfaces 2a and 2b of the circuit board 2 in the manner of the plane symmetry as described above, the vibrations transferred from the capacitors to the circuit board are cancelled out with each other; and, therefore, the circuit board is prevented from being resonated by the vibrations from the capacitors and the development of audible sounds with high sound pressure levels can be considerably reduced.

Specifically, if the capacitor 1a mounted on the front surface 2a of the circuit board 2 vibrates due to the piezoelectric effects as described above, so does the other capacitor 1b mounted on the back surface 2b, as shown in Fig. 4. The vibrations due to the piezoelectric effects include such vibrations generated by various state variations as thickness mode vibrations, thickness shear mode vibrations, planar shear mode vibrations, torsion mode vibrations and 25 distortion mode vibrations. For the sake of illustration,

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however, only the thickness mode vibrations developed by the deformation along the direction normal to the surfaces of the circuit board 2 will be considered.

The capacitors 1a and 1b of the present invention would  
5 also generate vibrations as in prior-art capacitors. Since,  
however, the capacitors 1a and 1b mounted on the front and the  
back surface 2a and 2b of the circuit board 2 are of the  
substantially identical structures and are disposed on the  
substantially plane-symmetrical positions, directions Da1 and  
10 Da2 of state variations developed in the capacitor 1a is  
opposite to directions Db1 and Db2 of those in the other  
capacitor 1b.

Figs. 5A and 5B represent waveforms of vibrations  
generated from the capacitors 1a and 1b, respectively. The  
15 waveform of the capacitor 1a is phase-shifted from that of the  
capacitor 1b by 180 degrees. As a result, the vibrations  
transferred from the two capacitors 1a and 1b to the circuit  
board 2 are cancelled out with each other and the resonance  
of the circuit board 2 is prevented.

20 Therefore, sounds developed by the vibrations of the two  
capacitors 1a and 1b would not be amplified so that audible  
sounds of high sound pressure levels can be considerably  
reduced.

It should be noted that the embodiment of the invention  
25 described above is but one exemplary implementation of the  
prevention and that many other implementations may also be

contemplated to realize the present invention. For instance, even though the preferred embodiment of the invention has been described with reference to the DC-DC converter incorporating therein the capacitors of the invention, it will be apparent 5 to those skilled in the art that the present invention can be also implemented in other electronic circuits to obtain the same result. Electronic circuits which can incorporate the present invention to thereby exhibit significant effects of suppressing vibrations and audible sounds includes, but not 10 limited thereto, an electronic circuit in which voltages applied to the capacitors 1a and 1b are variable, especially an electronic circuit in which applied voltages are continuously varied, a smoothing circuit of a power supply circuit in which the capacitors 1a and 1b are used as 15 smoothing capacitors, and an electronic circuit in which frequencies of voltages applied to the capacitors 1a and 1b vary in the audible frequency band (20Hz ~ 20KHz).

Further, the present invention is not intended to be limited to the above embodiment which prevents the vibrations 20 from being generated by using two symmetrical capacitors 1a and 1b in lieu of a single capacitor of a prior art circuit.

For example, if two capacitors are used in different parts of a circuit and substantially identical voltages are applied thereto, the two capacitors can be disposed at the 25 substantially plane-symmetrical positions on two opposite surfaces of a circuit board as described above to thereby

suppress vibrations from being generated by the two capacitors.

Further, if two capacitors are used on two different circuits and substantially identical voltages are applied to  
5 the capacitors, it is also possible to suppress the vibrations generated by the capacitors by mounting these two capacitors at their substantially plane-symmetrical positions on front and back surfaces of a circuit board as described above.

While the present invention has been described with  
10 respect to the particular embodiments, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the spirit and scope of the invention as defined in the following claims.